FORESEE LPDDR4

NCLD4C1MA256M32
NCLD4C2MA512M32
NCLD4C2MA768M32
NCLD4C2MA001G32

Datasheet

Version: B2

2017.08.01

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Revision History

Revision Number	***Description***	***Revision Date***
B0	Initial release.	2017.06
B1	Add die information	2017.07
B2	Modification 2 place discrption	2017.08

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Features

- Ultra-low-voltage core and I/O power supplies
  - VDD1 = 1.70–1.95V; 1.8V nominal
  - VDD2/VDDQ = 1.06–1.17V; 1.10V nominal
- Frequency range
  - up to 1600 –10 MHz (data rate range: 3200–20 Mb/s/pin)
- 16n prefetch DDR architecture
- 2-channel partitioned architecture for low RD/WR energy and low average latency
- 8 internal banks per channel for concurrent opera- tion
- Single-data-rate CMD/ADR entry
- Bidirectional/differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL/WL)
- Programmable and on-the-fly burst lengths (BL =16, 32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Up to 12.8 GB/s per die (2 channels x 6.4 GB/s)
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS-compliant, "green" packaging
- Programmable VSSQ (ODT) termination

Options

- VDD1/VDD2: 1.8V/1.1V
- Array configuration
  - 256 Meg x 32 (2 channels x16 I/O)
  - 512 Meg x 32 (2 channels x16 I/O)
  - 768 Meg x 32 (2 channels x16 I/O)
  - 1024 Meg x 32 (2 channels x8 I/O x 2)
- Device configuration
  - 256M16 x 2 channel x 1 die
  - 256M16 x 2 channel x 2 die
  - 256M16 x 2 channel x 3 die
  - 512M8 x 2 channel x 4 die
- FBGA "green" package
  - 200-ball VFBGA (10mm x 14.5mm x 0.95mm)
- Speed grade, cycle time
  - 625ps @ RL = 28/32 (x16 device)
  - 625ps @ RL = 32/36 (x8 device)
- Operating temperature range
  - –30°C to +85°C

- Revision
  - B1

Table 1: Key Timing Parameters

Part Number	Array configuration	Device Type	Clock Rate (MHz)	Data Rate (Mb/s/pin)	WRITE Latency		READ Latency	
					Set A	Set B	DBI Disabled	DBI Enabled
NCLD4C1MA256M32	256Mb x 32	x16 device	1600	3200	14	26	28	32
NCLD4C2MA512M32	512Mb x 32							
NCLD4C2MA768M32	768Mb x 32							
NCLD4C2MA001G32	1024Mb x 32	x8 device	1600	3200	14	26	32	36

SDRAM Addressing

The table below shows the addressing for the 8Gb die density. Where applicable, a distinction is made between per-channel and per-die parameters. All bank, row, and column addresses are shown per-channel.

Table 2: Device Addressing

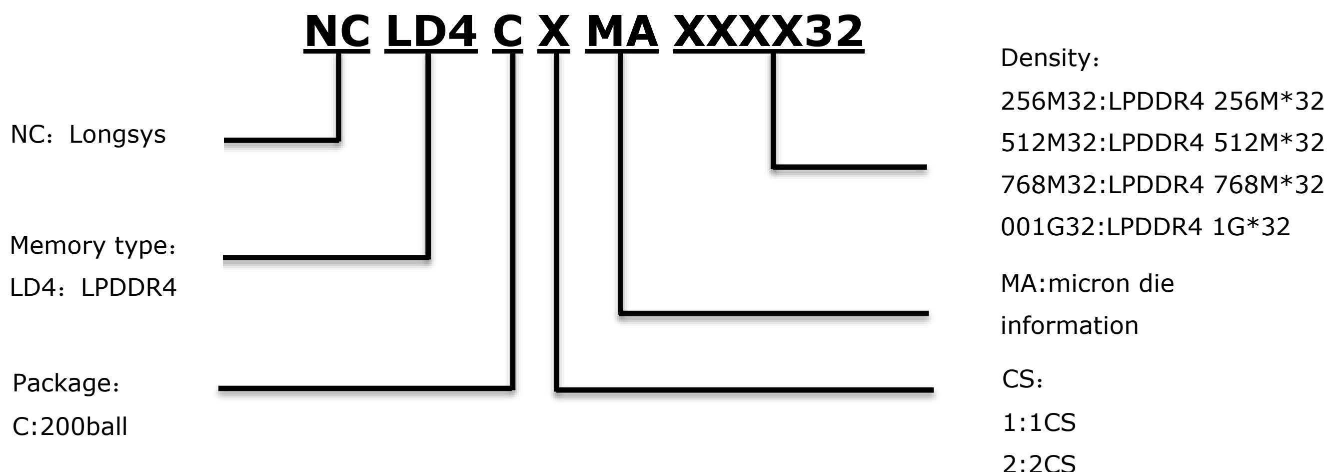
Configuration	256M32 (8Gb)	512M32	768M32	1024M32
Die per package	1	2	3	4
Device density (per die)	8Gb	8Gb	8Gb	8Gb
Device density (per channel)	4Gb	8Gb	12Gb	16Gb
Configuration	32Mb x 16 DQ x 8 banks x 2channels x 1 rank	32Mb x 16 DQ x 8 banks x 2channels x 2 ranks	64Mb x8 DQ x 8banks x 2 channels x 2 ranks + 32Mb x 16 DQ x 2 channels x 1rank	64Mb x 8 DQ x 8 banks x 2 channels x 2 ranks x 2
Number of channels (per die)	2	2	2	2
Number of ranks per channel	1	2	1(16DQ)/2(8DQ)	2
Number of banks (per channel)	8	8	8	8

Array prefetch (bits)(per channel)		256	256	192	128
Number of rows (per bank)		32,768	32,768	65536(8DQ)/32768 (16DQ)	65,536
Number of columns (fetch boundaries)		64	64	32(8DQ)/64(16DQ)	32
Page size (bytes)		2048	2048	1024(8DQ)/2048 (16DQ)	1024
Channel density (bits per channel)		4,294,967,296	8,589,934,592	12,884,901,888	17,179,869,184
Total density (bits per die)		8,589,934,592	8,589,934,592	8,589,934,592	8,589,934,592
Bank address		BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]
x16	Row	R[14:0]	R[14:0]	R[14:0]	–
	Column	C[9:0]	C[9:0]	C[9:0]	–
x8	Row	–	–	R[15:0]	R[15:0]
	Column	–	–	C[9:0]	C[9:0]
Burst starting		64-bit	64-bit	64-bit	64-bit

Notes:

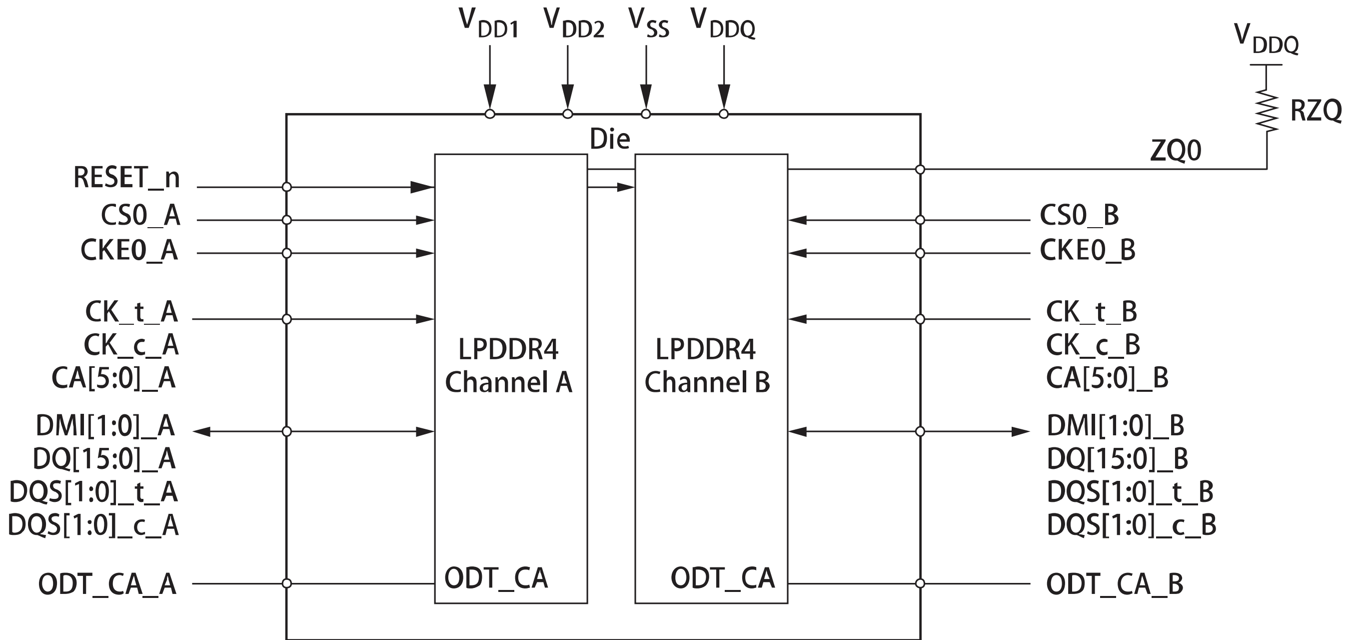
1. The lower two column addresses (C0–C1) are assumed to be zero and are not transmitted on the CA bus.
2. Row and column address values on the CA bus that are not used for a particular density are "Don't Care."
3. Refer to Byte Mode section for further information about 1024M32 (32Gb) configuration.

LPDDR4 Part Number Decode

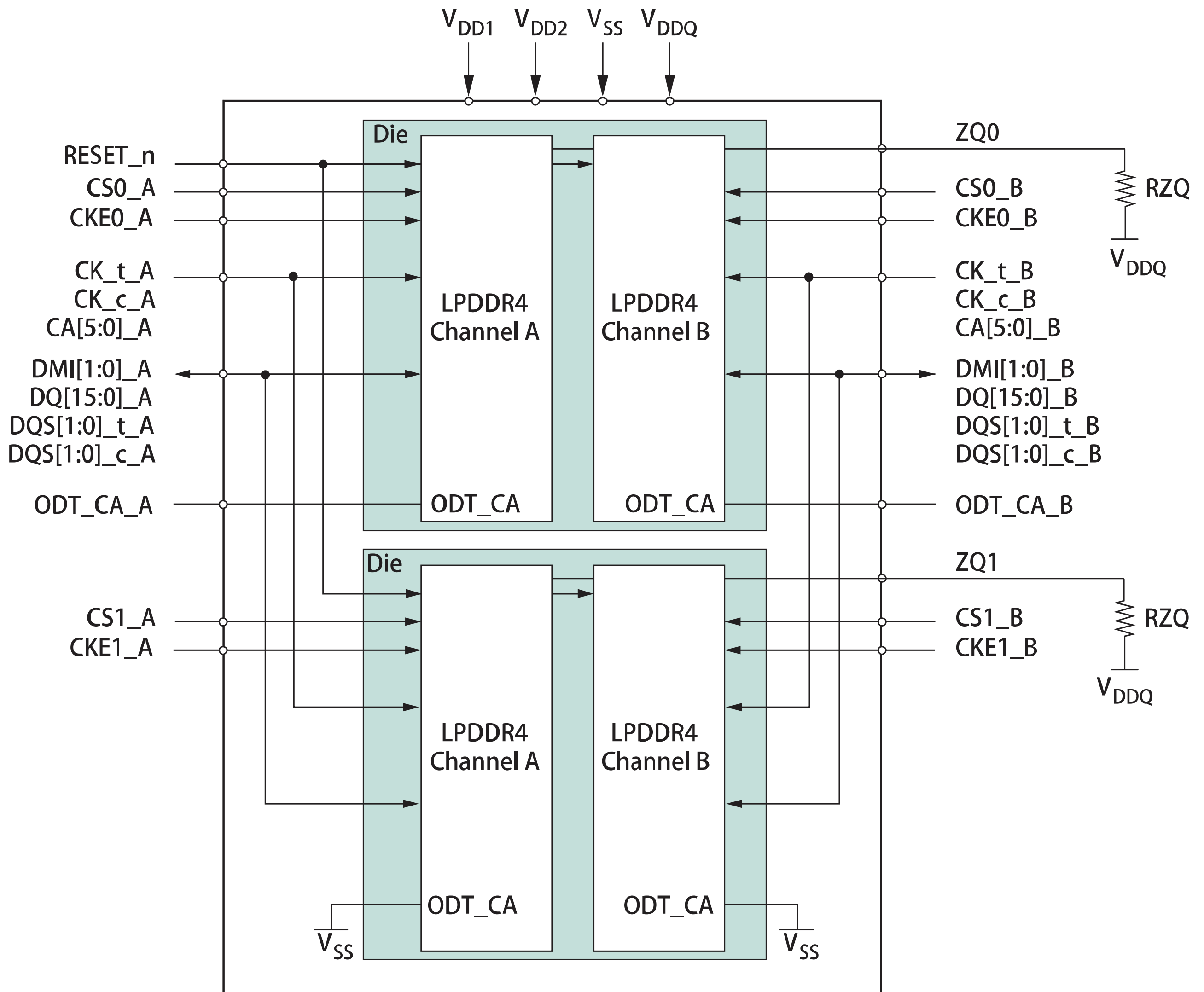


Package Block Diagrams

Single-Die, Dual-Channel Package Block Diagram



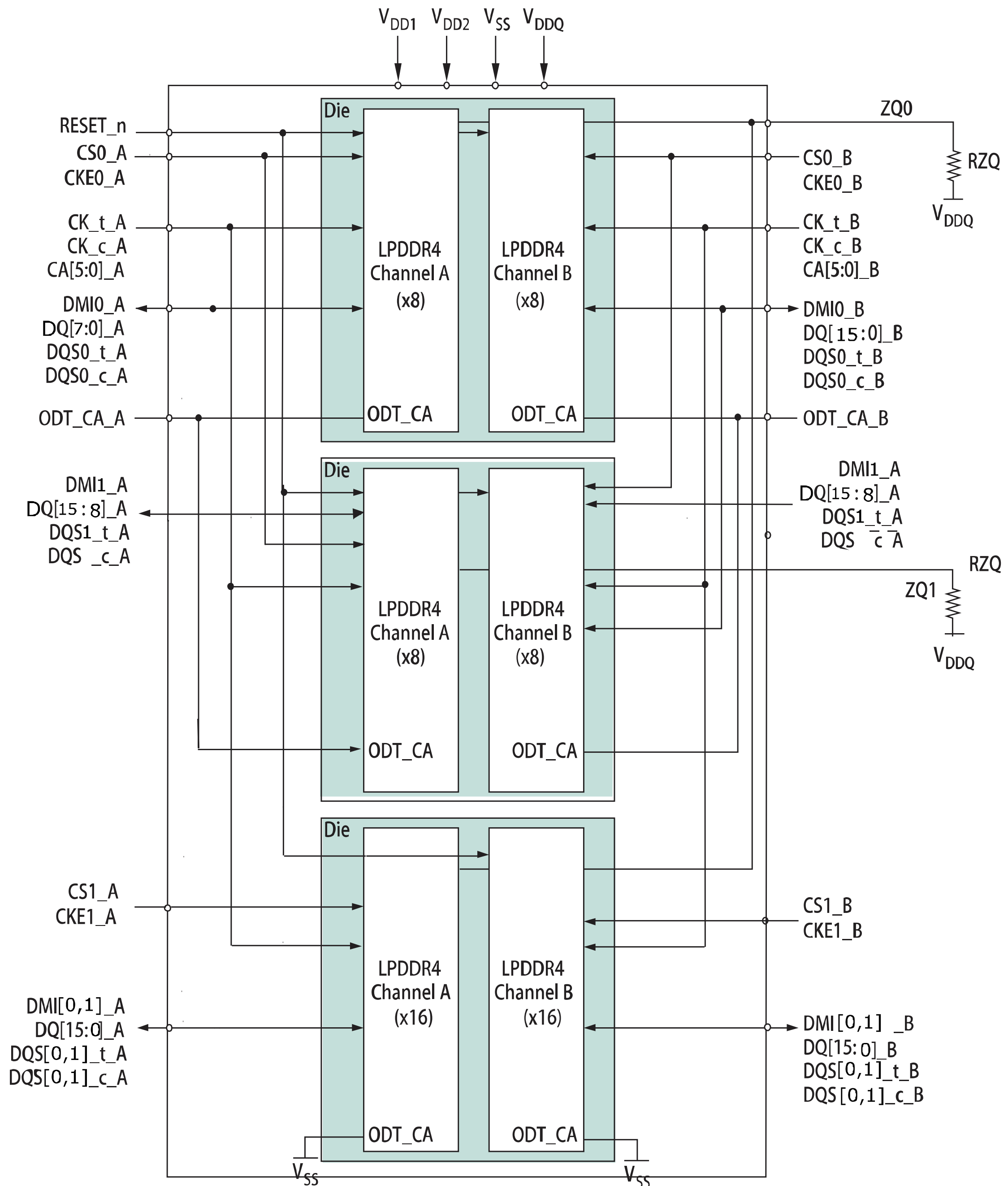
Dual-Die, Dual-Channel Package Block Diagram



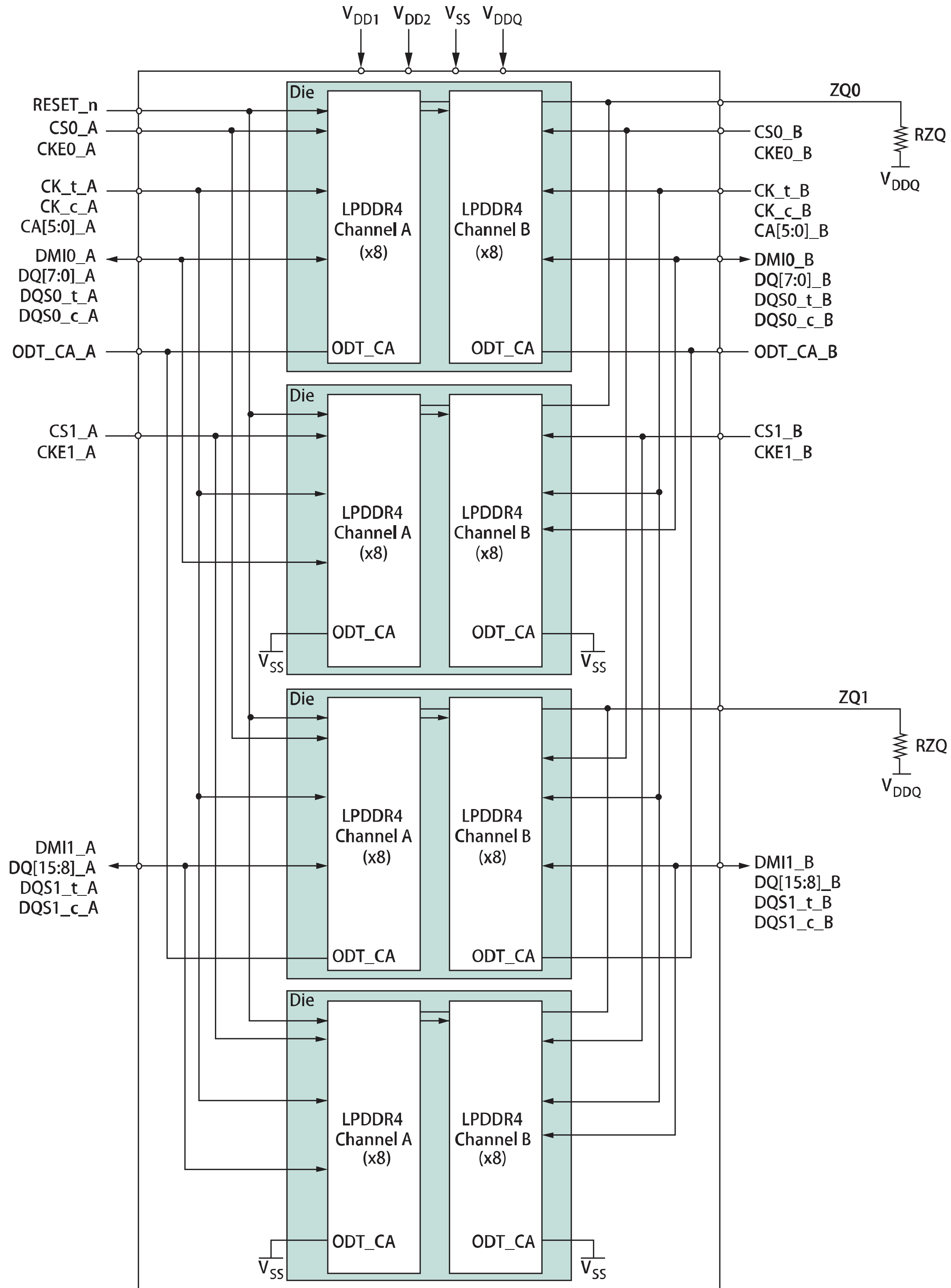
Note:

1. ODT_CA for Rank 0 of each channel is wired to the respective ODT ball. ODT_CA for Rank 1 of each channel is wired to V_{SS} in the package.

3-die，Dual-Channel Package Block Diagram



Quad-Die, Dual-Channel Package Block Diagram



Note：

1. ODT_CA for Rank 0 of each channel is wired to the respective ODT ball. ODT_CA for Rank 1 of each channel is wired to V_{SS} in the package.

Ball Assignments and Descriptions

200-Ball Dual-Channel Discrete VFBGA

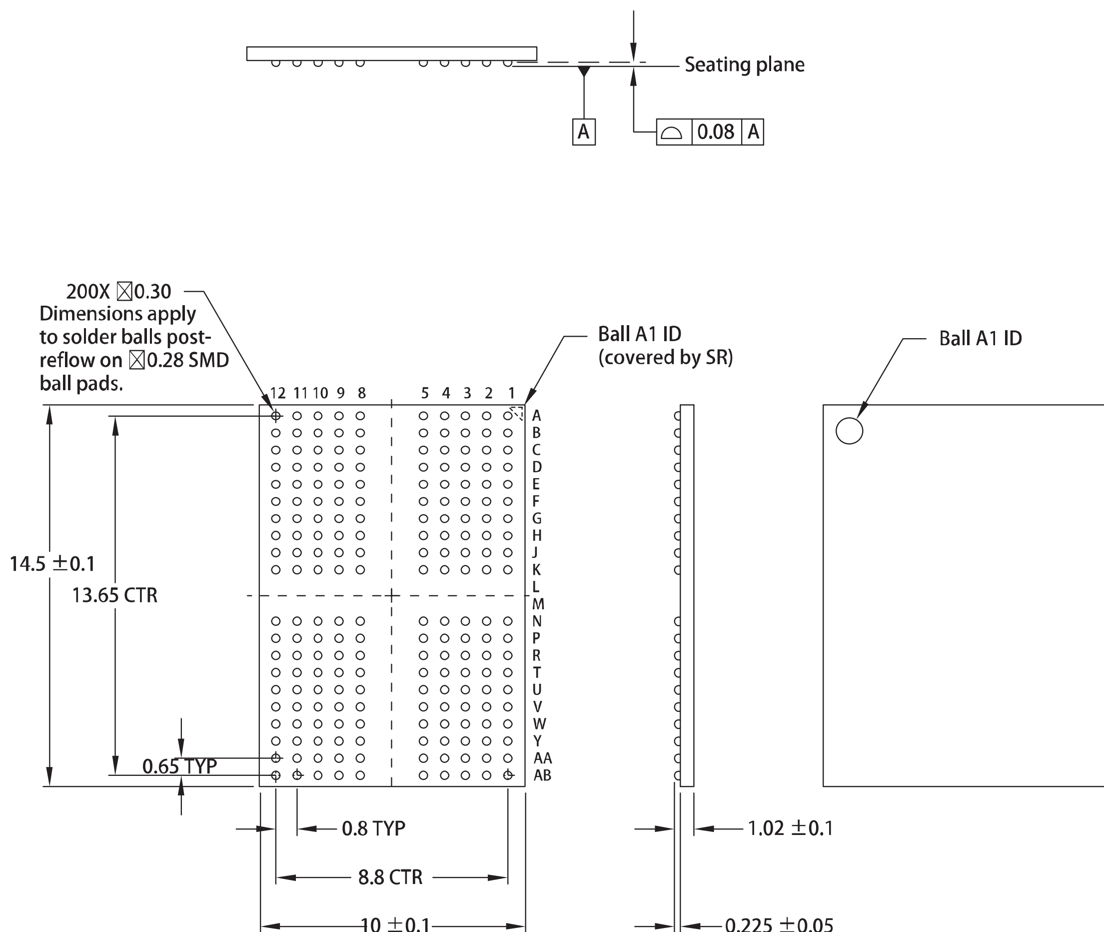
	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	VSS	VDD2	ZQ0			ZQ1	VDD2	VSS	DNU	DNU
B	DNU	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	DNU
C	VSS	DQ1_A	DMI0_A	DQ6_A	VSS			VSS	DQ14_A	DMI1_A	DQ9_A	VSS
D	VDDQ	VSS	DQS0_T_A	VSS	VDDQ			VDDQ	VSS	DQS1_T_A	VSS	VDDQ
E	VSS	DQ2_A	DQS0_C_A	DQ5_A	VSS			VSS	DQ13_A	DQS1_C_A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1
G	VSS	ODT_CA_A	VSS	VDD1	VSS			VSS	VDD1	VSS	ZQ2	VSS
H	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2
J	VSS	CA1_A	VSS	CKE0_A	CKE1_A			CK_t_A	CK_c_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	CS2_A			CKE2_A	VSS	VDD2	VSS	VDD2
L												
M												
N	VDD2	VSS	VDD2	VSS	CS2_B			CKE2_B	VSS	VDD2	VSS	VDD2
P	VSS	CA1_B	VSS	CKE0_B	CKE1_B			CK_T_B	CK_C_B	VSS	CA5_B	VSS
R	VDD2	CA0_B	CS1_B	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2
T	VSS	ODT_CA_B	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_N	VSS
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
V	VSS	DQ2_B	DQS0_C_B	DQ5_B	VSS			VSS	DQ13_B	DQS1_C_B	DQ10_B	VSS
W	VDDQ	VSS	DQS0_T_B	VSS	VDDQ			VDDQ	VSS	DQS1_T_B	VSS	VDDQ
Y	VSS	DQ1_B	DMI0_B	DQ6_B	VSS			VSS	DQ14_B	DMI1_B	DQ9_B	VSS
AA	DNU	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	DNU
AB	DNU	DNU	VSS	VDD2	VSS			VSS	VDD2	VSS	DNU	DNU

Ball/Pad Descriptions

Symbol	Type	Description
CK_t_A, CK_c_A,CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel (A, B) has its own clock pair.
CKE0_A, CKE1_A,CKE0_B, CKE1_B	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK.
CS0_A, CS1_A, CS0_B,CS1_B	Input	Chip select: Each channel (A, B) has its own CS signals.
CA[5:0]_A, CA[5:0]_B	Input	Command/address inputs: Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals.
ODT_CA_A, ODT_CA_B	Input	CA ODT Control: The ODT_CA pin is used in conjunction with the mode register to turn on/off the on-die termination for CA pins. It is bonded to V_{DD2} within the package,or at the package ball, for the terminating rank, and the non-terminating ranks are bonded to V_{SS} (or left floating with a weak pull-down on the DRAM die). The terminating rank is the DRAM that terminates the CA bus for all die on the same channel.
DQ[15:0]_A, DQ[15:0]_B	I/O	Data input/output: Bidirectional data bus.
DQS[1:0]_t_A,DQS[1:0]_c_A, DQS[1:0]_t_B,DQS[1:0]_c_B	I/O	Data strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes.
DMI[1:0]_A,DMI[1:0]_B	I/O	Data Mask/Data Bus Inversion: DMI is a dual use bi-directional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion (DBI),the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of

		data has a DMI signal. Each channel has its Own DMI signals.
ZQ0, ZQ1	Reference	ZQ Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to V_{DDQ} through a 240Ω ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2}	Supply	Power supplies: Isolated on the die for improved noise immunity.
V_{SS}	Supply	Ground Reference: Power supply ground reference.
RESET_n	Input	RESET: When asserted LOW, the RESET pin resets both channels of the die.
DNU	-	Do not use: Must be grounded or left floating.
NC	-	No connect: Not internally connected.

Package Dimensions



Notes:

1. All dimensions are in millimeters.
2. The package height does not include room temperature warpage.

I_{DD} Specification Parameters and Operating Conditions

Single Die Parameter

Parameter/Condition	Symbol	PowerSupply	Current	Notes
Operating one bank active-precharge current: ^{t}CK=^{t}CK(MIN);^{t}RC=^{t}RC(MIN); CKE is HIGH; CS is LOW between valid commands;CA bus inputs are switching; Data bus inputs are stable;ODT is disabled	I_{DD01}	V_{DD1}	7mA	
	I_{DD02}	V_{DD2}	80mA	
	I_{DD0Q}	V_{DDQ}	1.5mA	2
Idle power-down standby current:^{t}CK = ^{t}CK (MIN); CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching;Data bus inputs are stable; ODT is disabled	I_{DD2P1}	V_{DD1}	2mA	
	I_{DD2P2}	V_{DD2}	3.5mA	
	I_{DD2PQ}	V_{DDQ}	1.5mA	2
Idle power-down standby current with clock stop: CK_t =LOW, CK_c = HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD2PS1}	V_{DD1}	2mA	
	I_{DD2PS2}	V_{DD2}	3.5mA	
	I_{DD2PSQ}	V_{DDQ}	1.5mA	2
Idle non-power-down standby current: ^{t}CK = ^{t}CK (MIN); CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching;Data bus inputs are stable; ODT is disabled	I_{DD2N1}	V_{DD1}	2mA	
	I_{DD2N2}	V_{DD2}	45mA	
	I_{DD2NQ}	V_{DDQ}	1.5mA	2
Idle non-power-down standby current with clock stopped:CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD2NS1}	V_{DD1}	2mA	
	I_{DD2NS2}	V_{DD2}	25mA	
	I_{DD2NSQ}	V_{DDQ}	1.5mA	2
Active power-down standby current: ^{t}CK = ^{t}CK (MIN); CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching;Data bus inputs are stable; ODT is disabled	I_{DD3P1}	V_{DD1}	2mA	
	I_{DD3P2}	V_{DD2}	10mA	
	I_{DD3PQ}	V_{DDQ}	1.5mA	2
Active power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD3PS1}	V_{DD1}	2mA	
	I_{DD3PS2}	V_{DD2}	10mA	
	I_{DD3PSQ}	V_{DDQ}	1.5mA	3
Active non-power-down standby current: ^{t}CK = ^{t}CK (MIN);CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD3N1}	V_{DD1}	4mA	
	I_{DD3N2}	V_{DD2}	57mA	
	I_{DD3NQ}	V_{DDQ}	1.5mA	3
Active non-power-down standby current with clock stopped: CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	I_{DD3NS1}	V_{DD1}	4mA	
	I_{DD3NS2}	V_{DD2}	40mA	
	I_{DD3NSQ}	V_{DDQ}	1.5mA	3
Operating burst READ current: ^{t}CK = ^{t}CK (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL(MIN); CA bus inputs are switching; 50% data change each bursttransfer; ODT is disabled	I_{DD4R1}	V_{DD1}	5mA	
	I_{DD4R2}	V_{DD2}	450mA	
	I_{DD4RQ}	V_{DDQ}	270mA	4
Operating burst WRITE current: ^{t}CK = ^{t}CK (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL =WL(MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	I_{DD4W1}	V_{DD1}	5mA	
	I_{DD4W2}	V_{DD2}	350mA	
	I_{DD4WQ}	V_{DDQ}	100mA	3
	I_{DD51}	V_{DD1}	20mA	

All-bank REFRESH burst current: ${}^{t}CK = {}^{t}CK$ (MIN); CKE is HIGHbetween valid commands; ${}^{t}RC = {}^{t}RFCab$ (MIN); Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD52}	V_{DD2}	170mA	
	I_{DD5Q}	V_{DDQ}	1.5mA	3
All-bank REFRESH average current: ${}^{t}CK = {}^{t}CK$ (MIN); CKE is High between valid commands ${}^{t}RC = {}^{t}REFI$; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD5AB1}	V_{DD1}	4mA	
	I_{DD5AB2}	V_{DD2}	60mA	
	I_{DD5ABQ}	V_{DDQ}	1.5mA	3
Per-bank REFRESH average current: ${}^{t}CK = {}^{t}CK$ (MIN); CKE is High between valid commands ${}^{t}RC = {}^{t}REFI$; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	I_{DD5PB1}	V_{DD1}	4mA	
	I_{DD5PB2}	V_{DD2}	60mA	
	I_{DD5PBQ}	V_{DDQ}	1.5mA	3
Power-down self refresh current: CK_t = LOW, CK_c = HIGH;CKE is LOW; CA bus inputs are stable; Data bus inputs are stable;Maximum 1x self refresh rate; ODT is disabled(25℃)	I_{DD61}	V_{DD1}	0.4mA	5,6
	I_{DD62}	V_{DD2}	0.7mA	5,6
	I_{DD6Q}	V_{DDQ}	0.1mA	3,5,6

Notes:

1. ODT disabled: MR11[2:0] = 000b.
2. I_{DD} current specifications are tested after the device is properly initialized.
3. Measured currents are the summation of V_{DDQ} and V_{DD2}.
4. Guaranteed by design with output load = 5pF and R_{ON} = 40 ohm.
5. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh before going into the elevated temperature range.
6. This is the general definition that applies to full-array self refresh.
7. For all I_{DD} measurements, $V_{IHCKE} = 0.8 \times V_{DD2}$; $V_{ILCKE} = 0.2 \times V_{DD2}$.

Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Notes
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	-0.4	2.1	v	1
V_{DD2} supply voltage relative to V_{SS}	V_{DD2}	-0.4	1.5	v	1
V_{DDQ} supply voltage relative to V_{SS}	V_{DDQ}	-0.4	1.5	v	1
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	1.5	v	
Storage temperature	T_{STG}	-55	125	℃	2

Notes:

1. For information about relationships between power supplies, see the Voltage Ramp and Device Initialization section.
2. Storage temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JESD51-2 standard.

Recommended DC Operating Conditions

Symbol	Min	Typ	Max	DRAM	Unit	Notes
V_{DD1}	1.7	1.8	1.95	Core 1 power	V	1,2
V_{DD2}	1.06	1.1	1.17	Core 2 power/Input buffer power	V	1,2,3
V_{DDQ}	1.06	1.1	1.17	I/O buffer power	V	2,3

Notes:

1. VDD1 uses significantly less power than VDD2.
2. The voltage range is for DC voltage only. DC voltage is the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.
3. The voltage noise tolerance from DC to 20 MHz exceeding a peak-to-peak tolerance of 45mV at the DRAM ball is not included in the TdIVW.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{REF(CA),max_r0}$	$V_{REF(CA)}$ range-0 MAX operating point	30%	-	-	V_{DD2}	1,11
$V_{REF(CA),min_r0}$	$V_{REF(CA)}$ range-0 MIN operating point			10%	V_{DD2}	1,11
$V_{REF(CA),max_r1}$	$V_{REF(CA)}$ range-1 MAX operating point	42%			V_{DD2}	1,11
$V_{REF(CA),min_r1}$	$V_{REF(CA)}$ range-1 MIN operating point			22%	V_{DD2}	1,11
$V_{REF(CA),step}$	$V_{REF(CA)}$ step size	0.30%	0.40%	0.50%	V_{DD2}	2
$V_{REF(CA),set_tol}$	$V_{REF(CA)}$ set tolerance	-1.00%	0.00%	1.00%	V_{DD2}	3,4,6
		-0.10%	0.00%	0.10%	V_{DD2}	3,5,7
^{t}VREF_TIME-SHORT	$V_{REF(CA)}$ step time			100	ns	8
^{t}VREF_TIME-MIDDLE				200	ns	12
tVREF_TIME-LONG				500	ns	9
$^{t}V_{REF_time_weak}$				1	ms	13,14
$V_{REF(CA)_val_tol}$	$V_{REF(CA)}$ valid tolerance	-0.10%	0.00%	0.10%	V_{DD2}	10

Notes:

1. $V_{REF(CA)}$ DC voltage referenced to $V_{DD2(DC)}$.
2. $V_{REF(CA)}$ step size increment/decrement range. $V_{REF(CA)}$ at DC level.
3. $V_{REF(CA)}$,new = $V_{REF(CA)}$,old + n × $V_{REF(CA),step}$; n = number of steps; if increment, use "+"; if decrement, use "-".
4. The minimum value of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new}$ - 1.0% × V_{DD2}. The maximum value of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new}$ + 1.0% × V_{DD2}. For n > 4.
5. The minimum value of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new}$ - 0.10% × V_{DD2}. The maximum value of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new}$ + 0.10% × V_{DD2}. For n < 4.
6. Measured by recording the minimum and maximum values of the $V_{REF(CA)}$ output over the range, drawing a straight line between those points and comparing all other $V_{REF(CA)}$ output settings to that line.
7. Measured by recording the minimum and maximum values of the $V_{REF(CA)}$ output across four consecutive steps (n = 4), drawing a straight line between those points and comparing all other $V_{REF(CA)}$ output settings to that line.
8. Time from MRW command to increment or decrement one step size for $V_{REF(CA)}$.
9. Time from MRW command to increment or decrement $V_{REF,min}$ to $V_{REF,max}$ or $V_{REF,max}$ to $V_{REF,min}$ change across the $V_{REF(CA)}$ range in V_{REF} voltage.
10. Only applicable for DRAM component level test/characterization purposes. Not applicable for normal mode of operation. V_{REF} valid is to qualify the step times which will be characterized at the component level.
11. DRAM range-0 or range-1 set by MR12 OP[6].
12. Time from MRW command to increment or decrement more than one step size up to a full range of VREF voltage within the same $V_{REF(CA)}$ range.

13. Applies when VRCG high current mode is not enabled, specified by MR13 [OP3] = 0b.
14. $^{t}V_{REF}$_time_weak covers all $V_{REF(CA)}$ range and value change conditions are applied to $^{t}V_{REF}$_TIME-SHORT/MIDDLE/LONG.

Initialization Timing Parameters

Parameter	Min	Max	Unit	Comment
tINIT0	-	20	ms	Maximum voltage ramp time
tINIT1	200	-	μs	Minimum RESET_n LOW time after completion of voltage ramp
tINIT2	10	-	ns	Minimum CKE LOW time before RESET_n goes HIGH
tINIT3	2	-	ms	Minimum CKE LOW time after RESET_n goes HIGH
tINIT4	5	-	tCK	Minimum stable clock before first CKE HIGH
tINIT5	2	-	μs	Minimum idle time before first MRW/MRR command
tCKb	Note 1, 2	Note 1, 2	ns	Clock cycle time during boot

Notes:

1. Minimum tCKb guaranteed by DRAM test is 18ns.
2. The system may boot at a higher frequency than dictated by minimum tCKb. The higher boot frequency is system dependent.

AC Timing

Clock Timing

Parameter	Symbol	Min/ Max	Data Rate				Unit
			1600	2133	2667	3200	
Average clock period	^{t}CK(avg)	Min	1250	937	750	625	ps
		Max	100	100	100	100	ns
Average HIGH pulse width	^{t}CH(avg)	Min	0.46				^{t}CK(avg)
		Max	0.54				
Average LOW pulse width	^{t}CL(avg)	Min	0.46				^{t}CK(avg)
		Max	0.54				
Absolute clock period	^{t}CK(abs)	Min	tCK(avg)min + tJIT(per)min				ps
Absolute clock HIGH pulse width	^{t}CH(abs)	Min	0.43				^{t}CK(avg)
		Max	0.57				
Absolute clock LOW pulse width	^{t}CL(abs)	Min	0.43				^{t}CK(avg)
		Max	0.57				
Clock period jitter	^{t}JIT(per)allowed	Min	- 70	TBD	TBD	-40	ps
		Max	70	TBD	TBD	40	
Maximum clock jitter between two consecutiveclock cycles (includes clockperiod jitter)	^{t}JIT(cc)allowed	max	140	TBD	TBD	80	ps

Read Output Timing

Parameter	Symbol	Min/ Max	Data Rate 1600	2133	2667	3200	Unit
DQS output access time from CK_t/CK_c	^{t}DQSCK	Min	1500				ps
		Max	3500				
DQS output access time from CK_t/CK_c – voltage variation	^{t}DQSCK_VOLT	Max	7				ps/mV
DQS output access time from CK_t/CK_c–temperature variation	^{t}DQSCK_TEMP	Max	4				ps°/C
CK to DQS rank to rank variation	^{t}DQSCK_rank2rank	Max	1.0				ns
DQS_t, DQS_c to DQ skew total, per group, per access (DBI Disabled)	^{t}DQSQ	Max	0.18				UI
DQ output hold time total from DQS_t, DQS_c (DBI Disabled)	tQH	Min	MIN(tQSH, tQSL)				ps
Data output valid window time total, per pin (DBI-Disabled)	^{t}QW_total	Min	0.75	0.73		0.68	UI
DQS_t, DQS_c to DQ skew total, per group, per access (DBI-Enabled)	^{t}DQSQ_DBI	Max	0.18				UI
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	^{t}QH_DBI	Min	MIN(^{t}QSH_DBI, ^{t}QSL_DBI)				ps
Data output valid window time total, per pin (DBI-Enabled)	^{t}QW_total_DBI	Min	0.75	0.73		0.68	UI
DQS_t, DQS_c differential output LOW time (DBI-Disabled)	^{t}QSL	Min	^{t}CL(abs) – 0.05				^{t}CK(avg)
DQS_t, DQS_c differential output HIGH time (DBI-Disabled)	^{t}QSH	Min	^{t}CH(abs) – 0.05				^{t}CK(avg)
DQS_t, DQS_c differential output LOW time (DBI-Enabled)	^{t}QSL-DBI	Min	^{t}CL(abs) – 0.045				^{t}CK(avg)
DQS_t, DQS_c differential output HIGH time (DBI-Enabled)	^{t}QSH-DBI	Min	^{t}CH(abs) – 0.045				^{t}CK(avg)
Read preamble	^{t}RPRE	Min	1.8				^{t}CK(avg)

Read postamble	$^{t}RPST$	Min	0.4 (or 1.4 if extra postamble is programmed in MR)	$^{t}CK(avg)$
DQS Low-Z from clock	$^{t}LZ(DQS)$	Min	(RL x ^{t}CK)+ $^{t}DQSCK(Min)$ - ($^{t}RPRE(Max)$ x ^{t}CK) - 200ps	ps
DQ Low-Z from clock	$^{t}LZ(DQ)$	Min	(RL x ^{t}CK) + $^{t}DQSCK(Min)$ - 200ps	ps
DQS High-Z from clock	$^{t}HZ(DQS)$	Min	(RL x ^{t}CK) + $^{t}DQSCK(Max)$+(BL/2 x ^{t}CK) + ($^{t}RPST(Max)$ xtCK) - 100ps	ps
DQ High-Z from clock	$^{t}HZ(DQ)$	Min	(RL x ^{t}CK) + $^{t}DQSCK(Max)$ + $^{t}DQSQ(Max)$ + (BL/2 x tCK) -100ps	ps

Write Timing

Parameter	Symbol	Min/ Max	Data Rate				Unit
			1600	2133	2667	3200	
Rx timing window total at VdIVW voltage levels	TdIVW_total	Max	0.22			0.25	UI
Rx timing window 1-bit toggle (at VdIVW voltage levels)	TdIVW_1-bit	Max	TBD				UI
DQ and DMI input pulse width (at V_{CENT_DQ})	TdIPW	Min	0.45				UI
DQ-to-DQS offset	$^{t}DQS2DQ$	Min	200				ps
		Max	800				
DQ-to-DQ offset	$^{t}DQDQ$	Max	30				ps
DQ-to-DQS offset emperature variation	tDQS2DQ_temp	Max	0.6				ps/°C
DQ-to-DQS offset voltage variation	tDQS2DQ_volt	Max	33				ps/50mV
WRITE command to first DQS transition	$^{t}DQSS$	Min	0.75				tCK(avg)
		Max	1.25				
DQS input HIGH-level width	$^{t}DQSH$	-	0.4				tCK(avg)
DQS input LOW-level width	$^{t}DQSL$	Min	0.4				tCK(avg)
DQS falling edge to CK setup time	^{t}DSS	Min	0.2				tCK(avg)
DQS falling edge from CK hold time	^{t}DSH	Min	0.2				tCK(avg)
Write postamble	$^{t}WPST$	Min	0.4 (or 1.4 if extra postamble is programmed in MR)				tCK(avg)
Write preamble	$^{t}WPRE$	Min	1.8				tCK(avg)